DESIGN OF A NOVEL FET FREQUENCY DOUBLER USING A HARMONIC BALANCE ALGORITHM

Rowan Gilmore (Member, IEEE)

Schlumberger
Houston, Tx. 77252

ABSTRACT The design of a wideband FET frequency doubler operating with a 4-8 GHz input bandwidth is described. The doubler and bandreject amplifier combination achieve an average conversion loss of 3.5 dB across the 8-16 GHz output band. The design method uses the harmonic balance algorithm implemented on an IBM PC-AT personal computer.

Introduction

FET frequency doublers are important components in microwave receivers. Wideband doublers minimize local oscillator requirements in phase-locked loops and tracking systems because they provide a simple means of generating higher frequency components.

Several design techniques for frequency doublers have previously been reported[1-4]. The design presented here uses single-gate MESFETs and standard MIC techniques, and uses the nonlinearity of the FET transconductance to achieve doubling. The circuit inherently rejects the fundamental frequency and odd-order harmonics over bandwidths greater than an octave. The bandwidth of the doubler is limited only by the bandwidth of the Lange couplers used at the FET input and output.

One difficulty in designing a doubler covering octave or greater bandwidths is that the highest frequency in the input band to be doubled will overlap with the desired (second harmonic) output of a lower frequency input. Consequently, the traditional approach of tuning the FET input to the fundamental frequency and detuning the FET output to the second harmonic frequency will result in compromised performance at the band edges.

The second design difficulty lies in optimizing the FET operating point to achieve maximum conversion efficiency, i.e. to optimize circuit interaction with the device nonlinearity. Tradeoffs between FET gain and harmonic conversion efficiency are difficult to characterize.

This paper describes how the harmonic balance technique can be used to synthesize the desired circuit and to set the device bias and RF operating point, and illustrates a novel circuit approach used to obtain inherently broadband operation. As an example, an 8 -16 GHz wideband frequency doubler with conversion gains of -1 to -5 dB over the octave bandwidth is presented.

The Standard Harmonic Balance Technique

The standard harmonic balance technique has been reported in many previous papers[5,6,7]. It is an iterative technique which seeks to match the frequency components (harmonics) of current flowing in a set of branches joining two subcircuits. The branches are chosen in such a way that nonlinear elements are partitioned into one subcircuit; and linear elements into the other. The branches at the linear - nonlinear interface connect the two circuits and define corresponding nodes; current flowing out of one circuit must equal that flowing into the other. Matching the frequency components in each branch is simply a statement of Kirchoff's first law, which is a continuity equation for current. The current at each branch is obtained by a process of iteration so that dependencies are satisfied for both the linear and nonlinear sides of the circuit.

The nonlinear circuit is generally represented by a nonlinear set of equations

$$i_J(t) = g(v_1(t), ..., v_N(t)) \qquad (1)$$

where g is an arbitrary nonlinear function (and can include differentiation and integration), and i_J and v_J the current and voltage respectively at the Jth of N branches. The dependent variables i_J are nonlinear functions of the independent variables v_J at some point in time T_s. Periodic, steady state operation is assumed so that integrals and derivatives at T_s may be determined.

The linear circuit may be represented by an N by $(N+M)$ matrix, obtained by standard linear circuit analysis programs such as Touchstone[8]. The M additional variables are the additional external nodes (or branches) at which applied voltages (or currents) are present. The linear circuit is analysed in the frequency domain so that the matrix must be calculated at each frequency component present in the circuit. In the case of an applied input signal which contains harmonically related components at $\omega, 2\omega, ...q\omega$, there will be $(q+1)$ matrices relating the independent variables at each branch to the dependent variables:

0149-645X/86/0000-0585$01.00 © 1986 IEEE

$$\begin{pmatrix} v_1(k\omega) \\ \vdots \\ v_N(k\omega) \end{pmatrix} = \begin{pmatrix} H_{11}(k\omega) & H_{12}(k\omega) & \dots & H_{1(N+M)}(k\omega) \\ H_{21}(k\omega) & H_{22}(k\omega) & \dots & H_{2(N+M)}(k\omega) \\ \vdots & \vdots & \ddots & \vdots \\ H_{N1}(k\omega) & H_{N2}(k\omega) & \dots & H_{N(N+M)}(k\omega) \end{pmatrix} \begin{pmatrix} i_1(k\omega) \\ \vdots \\ i_N(k\omega) \\ v_{N+1}(k\omega) \\ \vdots \\ v_{N+M}(k\omega) \end{pmatrix} \quad \text{for} \quad k = 0, 1, ...q \qquad (2)$$

where the $H_{ij}(k\omega)$ are impedance or transfer ratios depending on which of the variables are voltages and currents. The purpose of the harmonic balance program is to find a simultaneous solution to (1) and (2) for $v_1, v_2, ...v_N$, so that $i_1, i_2, ...i_N$ may be determined.

Equation (1) is stated in the time-domain ; equation (2) in the frequency-domain. Time to frequency conversion is achieved using the discrete Fourier transform (DFT). If estimates of $v_J(t)$ for $J = 1, ...N$ at some time T_s are substituted into (1), i_J can be found at time T_s. If this is done at time instants $T_s, 2T_s, ...LT_s$ an L-point sequence of time samples of i_J results. If the waveform contains only discrete frequencies which are spaced by integral multiples of ω, up to $q\omega$, one can set

$$T_s = \frac{2\pi}{(2q+1)\omega}$$

with $L = (2q+1)$ to satisfy the Nyquist criterion, and can extract the desired frequency components at ω from the L-point sequence by using the discrete Fourier transform.

An initial estimate must be made for i_J and v_J because they are not known *a priori*. Iteration between equations (1) and (2) is performed using the DFT to obtain the frequency components from the time samples obtained from equation (1) until a self-consistent set of variables (i.e. those which satisfy the current continuity equations) is attained.

The harmonic balance algorithm was implemented in FORTRAN on an IBM AT Personal Computer. The required memory for the algorithm was 120K, with an additional 70K needed when compiled with the physical FET model reported by Madjar and Rosenbaum[9]. Run time was approximately two minutes for each solution. This is the first report of a harmonic balance technique implemented on a desk-top personal computer. The strength of this implementation is that it allows complete nonlinear, steady-state analysis of circuit-device interactions at a computer work-station.

FET Frequency Doubler Design

Two considerations are important in the design of an FET doubler. The first is that conversion loss be as low as possible, and the second is that the fundamental signal be rejected. Using conventional approaches, this is particularly hard to achieve at 8 GHz for a 4-8 GHz doubler, as this frequency is both the doubled 4 GHz signal and a possible fundamental input.

The input and output circuits of the basic FET doubler stage were synthesized for maximum flat gain across the whole band, using standard small-signal techniques. The circuits can then be verified at small signal levels with the nonlinear algorithm and model. Unlike conventional single-frequency doublers however, the wideband input and output matching circuits must be low Q to maximize bandwidth. The FETs used were NE71000 Ku band FETs.

The circuit topology chosen is shown in Figure 1. Using the harmonic balance program, the (small-signal derived) matched FET stage was analyzed for doubling efficiency at various device bias and RF drive points. The model used has been previously reported[9,10], and contains a three-terminal nonlinear capacitance in addition to nonlinearities in g_m and g_D. Optimum conversion efficiency was obtained by setting the device bias near pinch-off, using an RF- bypassed 50 ohm resistance in the source. Biased in this fashion, the FET behaves as a matched rectifier. Modelled simulations of fundamental input and output power, and second harmonic generation at 8 GHz input are shown in Figure 2. When biased at $V_{GS} = -0.5V$ (Figure 2a), the FET gain is higher, but the second harmonic output is no better (at high input powers) than when biased at $V_{GS} = -1.0V$ (Figure 2b). Consequently, biasing the FET near pinchoff at -1 volt achieves better fundamental rejection without degradation of conversion efficiency. Both the fundamental and second harmonic frequencies undergo considerable gain expansion as the input power is increased. The classic 2:1 ratio in the rate of rise of the second harmonic to the fundamental does not occur at -1 V gate bias because the input signal does not lie completely within the

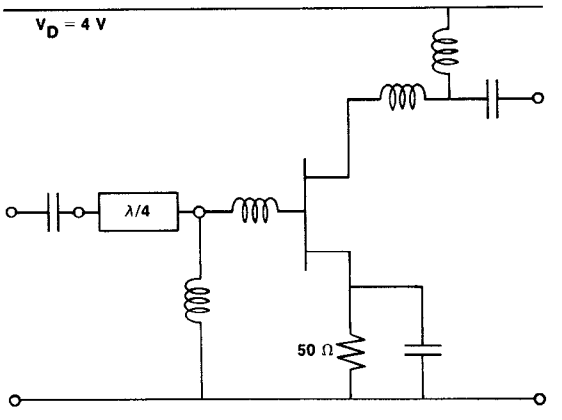

Figure 1. Circuit topology of the nonlinear FET element used with the broadband doubler.

square-law region of the FET. Harmonic generation and fundamental rejection is optimized with an input power of about 5 dBm. At input powers higher than this the gain of the fundamental frequency increases faster than the second harmonic, so that fundamental frequency rejection worsens.

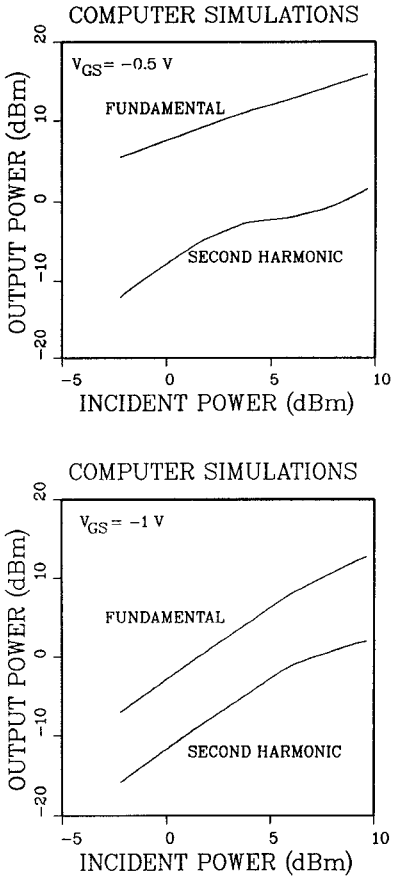

Figure 2. Modelled simulations of the nonlinear FET element of Figure 1. Computed fundamental and second harmonic output power are shown as a function of fundamental input power at

(a) $V_{GS} = -0.5V$

(b) $V_{GS} = -1.0V$

Circuit Topology

Although optimized for second harmonic generation, Figure 2b shows that the level of the fundamental frequency at the single-stage FET output is still approximately 10 dB greater than the desired second-harmonic. The single stage doubler just described has no rejection, because the use of high Q circuits to achieve fundamental frequency rejection would result in narrow bandwidth and poor conversion performance at the lower edge of the output band (which corresponds to the upper edge of the input band in an octave bandwidth design).

In this application, the FET is used only as a nonlinear element to generate the second harmonic. Any stable device with sufficient microwave gain could be used in place of the FET. For example, Schottky diodes could be substituted for the FETs in order to generate a second harmonic signal.

Fundamental frequency rejection can be achieved by two means:

(i) by coupling two FET half-wave rectifiers antisymmetrically, so that conduction occurs on alternate half cycles, as illustrated in Figure 3. Two Lange couplers, oriented to provide a total path difference of 180^0, are ideal for this purpose, as they allow isolation between the two half-circuits, and provide good input and output VSWR over the necessary bandwidth, in addition to the required phase difference. The antisymmetric configuration effectively nulls out the fundamental and odd-order harmonics, because the 180^0 phase shift difference results in pure cancellation (subtraction) of the odd-order frequencies .

(ii) by adding a following band-reject amplifier. Additional cancellation of the fundamental is achieved in this balanced amplifier stage, as its Lange couplers are designed for the midrange of the output band and reject the input band. In addition, the amplifier provides gain at the second harmonic and rejection at the fundamental. Standard small-signal techniques were used to synthesize this stage.

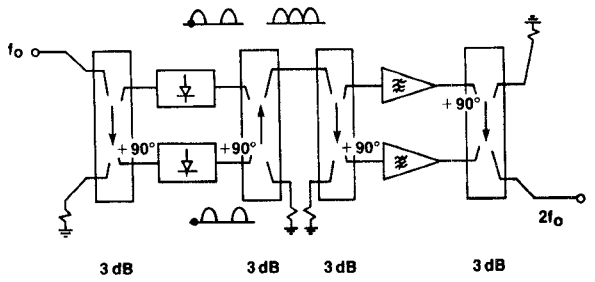

Figure 3. Construction of the broadband doubler. The initial block comprises a pair of nonlinear FET elements coupled by two antisymmetric Lange-couplers to provide a 180^0 path difference. The final block is a balanced band-pass amplifier that uses symmetrically coupled Lange couplers to provide zero net phase difference.

Doubler Results

The circuit in Figure 3 was fabricated on a .015" alumina substrate, and used Lange couplers centered at 12 GHz. The complete doubler is shown in Figure 4. Circuit size was 0.5" x 0.25", and power consumption was 60 mA at 4 V input.

Measured doubler results are illustrated in Figure 5. Input drive level of +5 dBm was found to give the highest conversion efficiency, close to that determined in the simulations. The second harmonic output power was tuned to rise slightly over the band to compensate for following system losses. At 16 GHz, peak output power of +4 dBm was

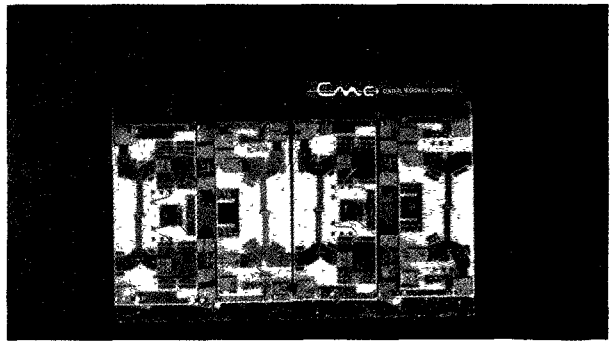

Figure 4. Photograph of the broadband doubler.

achieved, for a total conversion loss of 1 dB. Rejection at the fundamental frequency was then 20 dB. Maximum conversion loss of 5 dB was obtained at 8 GHz output, where fundamental frequency rejection was 15 dB. Fundamental rejection around 7 GHz was very high due to a resonance in the bias lines. The bias lines were left unmodified as they actually improved performance. This resonance is narrowband, and is indicative of the improvement in rejection that could be obtained by using higher Q circuits (but with consequent bandwidth reduction).

Conclusion

A technique that enables the investigation of device-circuit nonlinearities has been presented. Using modifications to an existing FET model, a harmonic balance method was devised which was efficiently implemented on an IBM PC-AT. As an example, the design of a novel FET frequency doubler covering octave bandwidths was presented. The harmonic balance method was used to set the device bias and operating points. The circuit structure is applicable with any microwave nonlinear device as the active element. Using single gate FETs, conversion efficiencies of from -1 to -5 dB were obtained across the output frequency band of 8 to 16 GHz.

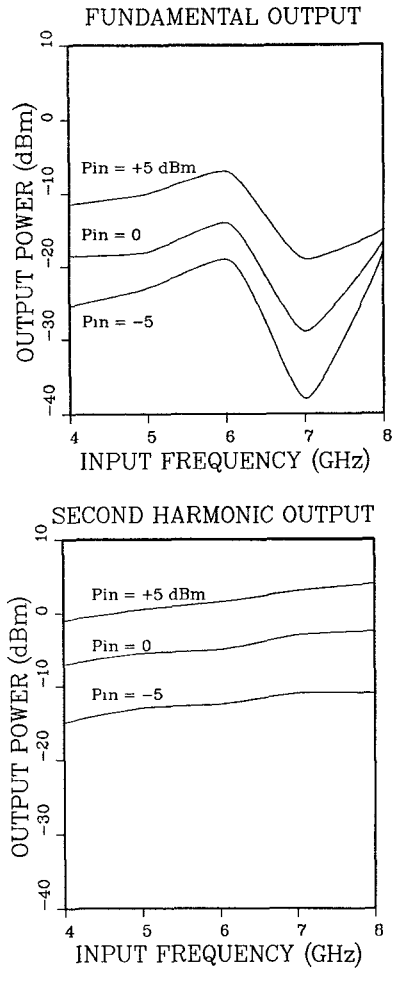

Figure 5. Experimental doubler results, showing the fundamental and second harmonic output power as a function of frequency, for input power levels of -5, 0, and +5 dBm.

Acknowledgements

The author wishes to acknowledge the support and encouragement of his doctoral advisor Prof. Fred Rosenbaum, as well as Don Green who developed many nonlinear modeling techniques at the Microwave Laboratory of Washington University. Thanks are also due to the author's previous employer, Central Microwave Co., and especially to Rick Kiehne, for their assistance in the experimental evaluation of the components discussed.

Bibliography

[1] C. Rauscher, "Frequency Doublers with GaAs FETs", IEEE Int. Microwave Symposium Digest, pp.280-282.

[2] R. Stancliff, "Balanced dual-gate GaAs FET frequency doublers", IEEE 1981 Int. Microwave Symposium Digest, pp. 143-145.

[3] E. Camargo et. al., "Sources of Nonlinearity in GaAs MESFET Frequency Multipliers", IEEE 1983 Int. Microwave Symposium Digest, pp.343-345.

[4] R. J. Gilmore, "Octave-bandwidth Microwave FET Doubler", Electronics Letters, Vol. 21, No. 12, pp.532-533, 6 June 1985.

[5] M. S. Nakhla and J. Vlach, "A Piecewise Harmonic Balance Technique for Determination of Periodic Response of Nonlinear Systems", IEEE Trans. on Circuits and Systems, Vol. CAS-23, No. 2, February 1976.

[6] V. Rizzoli, A. Lipparini, and E. Marazzi, "A General Purpose Program for Nonlinear Microwave Circuit Design", IEEE Trans. on Microwave Theory and Tech., Vol. MTT-31, No. 9, pp. 762-770, September 1983.

[7] D. R. Green and F. J. Rosenbaum, "Performance Limits on GaAs FET Large- and Small- Signal Circuits", Report N00014-80-0318, Washington University, St. Louis, Mo., October, 1981.

[8] EESOF, 31194 LaBaya Drive, Westlake Village, CA.

[9] A. Madjar and F. J. Rosenbaum, "A Large-Signal Model for the GaAs MESFET", IEEE Trans. on Microwave Theory and Tech., Vol. MTT-29, No. 8, pp.781-788, August 1981.

[10] R. J. Gilmore and F. J. Rosenbaum, "Circuit Design to Reduce Third Order Intermodulation Distortion in FET Amplifiers", IEEE 1985 Int. Microwave Symposium Digest, pp. 413-416.